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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,541	09/30/2003	Tetsuya Okada	2905-106	1842

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,541	OKADA ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *9-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/6/04, 7/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group 1 (claims 1-8 and 14-18) in the reply filed on 10/20/04 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

It is noted that the restriction requirement listed claim 18 as being part of the Group I invention. This was in error as claim 18 does not exist. The claims of Group I should correctly be listed as claims 1-8 and 14-17. Since Group I was elected, claims 1-8 and 14-17 are examiner herein.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. Figures 8A, 8B, 9A, 9B, 9C and 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the second reverse-conduction type semiconductor region formed **around** the semiconductor layer must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Product-by-Process Limitations

5. While not objectionable, the Office reminds Applicant that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wethheim,* 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al.,* 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. Note that applicant has the burden of proof in such cases, as the above case law makes clear. Thus, no patentable weight will be given to those process steps which do not add structural limitations to the final product.

Claim Objections

6. Claims 1-8 and 14-17 are objected to because of the following informalities:

a. Claims 1, 15 and 17 recite a second reverse-conduction type semiconductor region formed **around** the semiconductor layer. This limitation is objected to as the figures (figure 1A and 1B for example) show the second reverse-conduction type semiconductor region (labeled 4) having a ring shape and being formed **in** the semiconductor layer (labeled 2) with portions of the semiconductor layer 2 being

outside the ring-shaped second reverse-conduction type semiconductor region 4. Thus, the claim seems to be inconsistent with the structure shown in the figures. It is suggested that the limitation be amended to recite "a second reverse-conduction type semiconductor region formed **in** the semiconductor layer." Claims 2-8 depend from claim 1 and are thus similarly objected to as they contain all the limitations of the claims from which they depend.

b. Claims 4 and 14 recite the semiconductor layer is fully filled in a depletion layer and claim 16 recites means for fully filling the semiconductor layer in a depletion layer. This language is objected to as when a reverse voltage is applied a depletion layer is formed. The depletion layer is a result of the hole and electron carriers crossing the pn-junction under reverse bias and leaving behind a region that is "depleted" of carriers. Thus, the depletion region is not filled, but is by definition depleted or emptied. It is suggested that the limitations be amended to read that the semiconductor layer is "fully depleted" instead of fully filled in a depletion layer. Claims 15 and 17 depend from claims 14 and 16 and are thus similarly objected to as they contain all the limitations of the claims from which they depend. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. Claim 4 recites the limitation "the respective neighboring first reverse-conduction type semiconductor regions" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-8 and 14-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Sugita (EP 0 372 428 A1).

Sugita discloses a semiconductor device in figures 5-11B and on page 4 line 51 through page 7 line 55, for example. Specifically, Sugita discloses a semiconductor device comprising:

a one-conduction type semiconductor substrate 36 (figure 5);

a one-conduction type semiconductor layer 38,40,42 formed on the substrate 36 (figure 5; the one-conduction type semiconductor layer 38,40,42 is considered to be the portion inside region 48);

a plurality of first reverse-conduction type semiconductor regions 46 formed in the semiconductor layer 38,40,42 (figure 5);

a second reverse-conduction type semiconductor region 48 formed around the semiconductor layer 38,40,42 so as to surround the plurality of first reverse-conduction type semiconductor regions 46 (figure 5, region 48 is considered to "surround" the semiconductor layer 38,40,42 as the semiconductor layer is considered to be portion

inside of region 48; region 48 surrounds the plurality of first reverse-conduction type semiconductor regions 46 as disclosed on page 5 lines 14-16); and

a metal layer 34 forming Schottky junctions in cooperation with the semiconductor layer 38,40,42 and surfaces of the fist reverse-conduction type semiconductor regions 46 (figure 5; metal layer 34 is disclosed as being a Schottky-barrier metal on page 5 line 9; the metal layer 34 forms the claimed junctions as it contacts the top surface of both the N- and the P+ regions as in the instant application, see figure 1B of the instant application).

With regard to claims 2 and 3, the limitations recited in these claims are product-by-process limitations. Neither the process of burying reverse-conduction type semiconductor material into trenches formed in the semiconductor layer nor the process of diffusing reverse-conduction type impurities into the semiconductor layer necessarily results in a different structure than that disclosed by Sugita. Thus, the product-by-process limitations recited do not structurally distinguish the claims over the product disclosed by Sugita. Further, it is noted that Sugita does teach the specific method of claim 3 in that they teach diffusing impurities (by implantation) on page 5 lines 30-31.

With regard to claim 4, respective neighboring first reverse-conduction type semiconductor regions 46 are disposed so as to be spaced from one another at such intervals that the semiconductor layer 38,40,42 between neighboring first reverse-conduction type semiconductor regions is fully filled in a depletion layer when reverse voltages are applied (figure 9 shows depletion region 56 when a reverse voltage is

applied; this figure shows that regions 46 are arranged such that the semiconductor layer 38,40,42 between regions 46 is fully depleted when a reverse voltage is applied).

With regard to claim 5, respective neighboring first reverse-conduction type semiconductor regions 46 are disposed so as to be spaced apart from one another at substantially equal intervals (figure 5; see also figures 7A and 7B which show an enlarged portion showing regions 46 evenly spaced).

With regard to claim 6, the first reverse-conduction type semiconductor regions 46 are formed with a thickness smaller than the thickness of the semiconductor layer 38,40,42 (figure 5).

With regard to claims 7 and 8, the limitations recited in these claims are product-by-process limitations. Neither the process of diffusing the second reverse-conduction type semiconductor region nor the process of burying semiconductor material into a plurality of trenches formed in the semiconductor layer necessarily results in a different structure than that disclose by Sugita. Thus, the product-by-process limitations recited do not structurally distinguish the claims over the product disclosed by Sugita. Further, it is noted that Sugita does teach the second reverse-conduction type semiconductor region 48 is a diffusion region as it is formed by diffusing impurities (by implantation) on page 5 lines 30-31.

With regard to claim 14, Sugita discloses a semiconductor device comprising:

a one-conduction type semiconductor substrate 36 (figure 5);

a one-conduction type semiconductor layer 38,40,42 formed on the substrate 36 (figure 5; the one-conduction type semiconductor layer 38,40,42 is considered to be the portion inside region 48);

at least one reverse-conduction type semiconductor regions 46,48 formed in the semiconductor layer 38,40,42 (figure 5);

a metal layer 34 forming a Schottky junction area in cooperation with the semiconductor layer 38,40,42 and surfaces of the at least one reverse-conduction type semiconductor regions 46,48 (figure 5; metal layer 34 is disclosed as being a Schottky-barrier metal on page 5 line 9; the metal layer 34 forms the claimed junction are as it contacts the top surface of both the N- and the P+ regions as in the instant application, see figure 1B of the instant application); and

the at least one reverse-conduction type semiconductor region 46,48 is configured such that the semiconductor layer 38,40,42 in a Schottky junction area (the area inside region 48) is fully filled in a depletion layer when a reverse voltage is applied (figure 9 shows depletion region 56 when a reverse voltage is applied; this figure shows that regions 46,48 are configured such that the semiconductor layer 38,40,42 between regions 46,48 is fully depleted when a reverse voltage is applied).

With regard to claim 15, the at least one reverse-conduction type semiconductor region includes:

a plurality of first reverse-conduction type semiconductor regions 46 formed in the semiconductor layer (figure 5); and

a second reverse-conduction type semiconductor region 48 formed around the semiconductor layer 38,40,42 so as to surround the plurality of first reverse-conduction type semiconductor regions 46 (figure 5, region 48 is considered to "surround" the semiconductor layer 38,40,42 as the semiconductor layer is considered to be portion inside of region 48; region 48 surrounds the plurality of first reverse-conduction type semiconductor regions 46 as disclosed on page 5 lines 14-16).

With regard to claim 16, Sugita discloses a semiconductor device comprising:

a substrate 36 (figure 5);

a semiconductor layer 38,40,42 formed on the substrate 36 (figure 5; the semiconductor layer 38,40,42 is considered to be the portion inside region 48);

a metal layer 34 forming a Schottky junction area in cooperation with the semiconductor layer 38,40,42 (figure 5; metal layer 34 is disclosed as being a Schottky-barrier metal on page 5 line 9; the metal layer 34 forms the claimed junction are as it contacts the top surface of both the N- and the P+ regions as in the instant application, see figure 1B of the instant application); and

means for fully filling the semiconductor layer in the Schottky junction are in a depletion layer when a reverse voltage is applied such as to pinch off the semiconductor layer so as to suppress an IR leak current (the means are first 46 and second 48 reverse-conduction type semiconductor regions, figure 9 shows the fully depleted layer 56 when a reverse voltage is applied, the semiconductor layer is "pinched off" since the depletion layer around each region 46 is joined with the depletion region around the

adjacent region 46, suppressing an IR leak current is an inherent property of the device).

With regard to claim 17, the means for fully filling includes:

a plurality of first reverse-conduction type semiconductor regions 46 formed in the semiconductor layer (figure 5); and

a second reverse-conduction type semiconductor region 48 formed around the semiconductor layer 38,40,42 so as to surround the plurality of first reverse-conduction type semiconductor regions 46 (figure 5, region 48 is considered to "surround" the semiconductor layer 38,40,42 as the semiconductor layer is considered to be portion inside of region 48; region 48 surrounds the plurality of first reverse-conduction type semiconductor regions 46 as disclosed on page 5 lines 14-16).

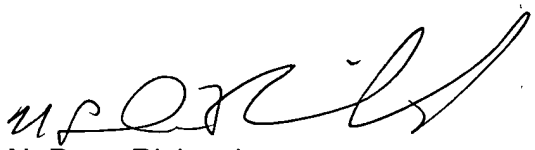
Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kan et al. (U.S. Patent No. 5345100), Mori et al. (U.S. Patent No. 5101244), Fujihira et al. (U.S. Patent No. 6175143 B1), Werner et al. (U.S. Patent No. 6184545 B1), Chang et al. (U.S. Patent No. 6426541 B2), Buchanan et al. (U.S. Patent No. 6462393 B2), Kaminski et al. (U.S. Patent No. 6501145 B1), Harada (U.S. Patent No. 6501146 B1), Buchanan et al. (U.S. Patent No. 6717229 B2), JP-2-137368, JP-3-105975, EP 0 435 105 A1.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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AU 2815